36. (ONCE AMENDED) A system according to Claim 32, wherein said receive memory has a watermark setting at which the port issues a start-of-packet interrupt to the communications processor.

REMARKS

Claims 1-42 remain in this application. Claims 33 and 36 have been amended.

Applicant thanks the Examiner for the detailed study of this application and the prior art. Applicant has amended the claims to correct the informality where the word "HDLC" is improperly used without proper antecedent basis.

Applicant also submits a Declaration Under 37 CFR 1.131 that conclusively shows that prior to June 19, 1998, the effective date of the cited U.S. Patent No. 6,195,720 to Abiven et al., Applicant conceived and reduced to practice the invention as described and claimed in this patent application in this country at the SGS-Thomson Microelectronics, Inc. (now STMicroelectronics, Inc.) plant in Carrollton, Texas.

Exhibit 1 with sheets 1-17 are evidence of the conception and reduction to practice of the invention. As noted in the attached sheets 1-17, the inventor originally conceived the invention of using a frame address notification as a signal interrupt to the host CPU such that all relevant address fields for a received frame were currently resident in memory. The frame could be processed by the address and look-up engine (ALE) and dispatched to its destination to provide a pipelining effect that allows routing to occur in parallel, while the remainder of the frame could still be

incoming off the network wire. The DMA burst-size could be selected and cause appropriate address fields to be a variable within the initial burst read of the frame. Any MAC-level header, IP addresses, or even TCP/UDP ports could be read into memory by having the CPA look into an incoming frame for routing. This overcame the drawbacks of classic store and forward (SF) architecture where the host device was obligated to wait until the entire frame had been read off the wire and ownership of the associated external memory buffer had been reassigned before routing could take place.

Sheets 1-7 show the basic method and system with the FIFO receive memory, network device, host processor, shared system memory and direct memory access unit as part of an HDLC device. The communications processor selects the amount of data to be transferred from the FIFO receive memory to the shared system memory based on the desired address field to be analyzed by the host processor.

Sheets 8-11 show different headers and a TCP/UDP datagram encapsulated in an IP and MAC layer frame as examples of headers that could be used in the present invention.

Sheets 12-17 further show my write-up and various notes setting forth basic aspects of the invention.

Sheets 15 and 16 show the receive interrupt event time line and frame address notification of the present invention with the DMA interrupts, respectively.

Sheet 17 shows the type of device in which Applicant implemented firmware for the present invention. That device was a four port, 32-bit, controller produced by STMicroelectronics as a SWIFT™ ST52T3 fast HDLC controller.

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_____/

Each of the dates deleted from the sheets of Exhibit A are prior to June 19, 1998.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version With Markings to Show Changes Made."**

Applicant contends that this case is now in condition for allowance based upon the submission of the Declaration Under 37 CFR 1.131 and the present Amendment.

If the Examiner has any questions or suggestions for placing this case in condition for allowance, the undersigned attorney would appreciate a telephone call.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: **DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE, WASHINGTON, DC 20231**, on this 5th day of August, 2002.

Julie Lalan

In re Patent Application of:
KASPER
Serial No. **09/163,925**
Filing Date: **09/30/1998**
_____/

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 33 and 36 have been amended as follows:

33. (ONCE AMENDED) A system according to Claim 32, and further comprising an interrupt bus connected between the FIFO receive memory and communications processor, wherein said [HDLC] ports include an interrupt generator for generating an interrupt to the communications processor along the bus.

36. (ONCE AMENDED) A system according to Claim 32, wherein said receive memory has a watermark setting at which the [HDLC] port issues a start-of-packet interrupt to the communications processor.